FIG. 1

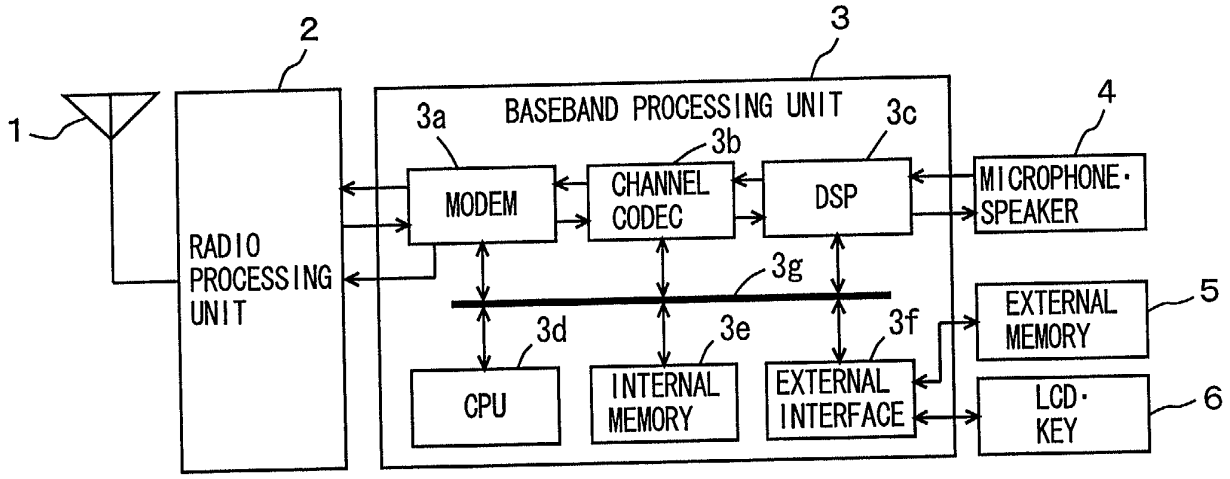

1
2
3
BASEBAND PROCESSING UNIT
3a
3b
3c
4
MODEM
CHANNEL CODEC
DSP
MICROPHONE· SPEAKER
RADIO PROCESSING UNIT
3g
EXTERNAL MEMORY
5
3d
3e
3f
CPU
INTERNAL MEMORY
EXTERNAL INTERFACE
LCD· KEY
6

FIG. 2

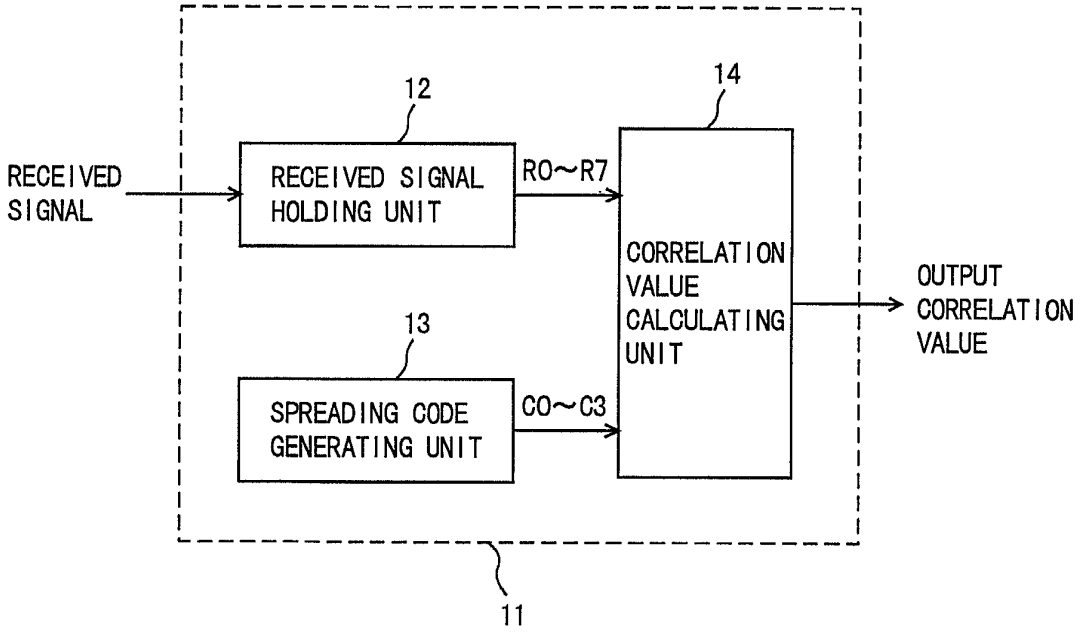

12
14
RECEIVED SIGNAL
RECEIVED SIGNAL HOLDING UNIT
R0~R7
CORRELATION VALUE CALCULATING UNIT
OUTPUT CORRELATION VALUE
13
SPREADING CODE GENERATING UNIT
C0~C3
11

FIG. 3

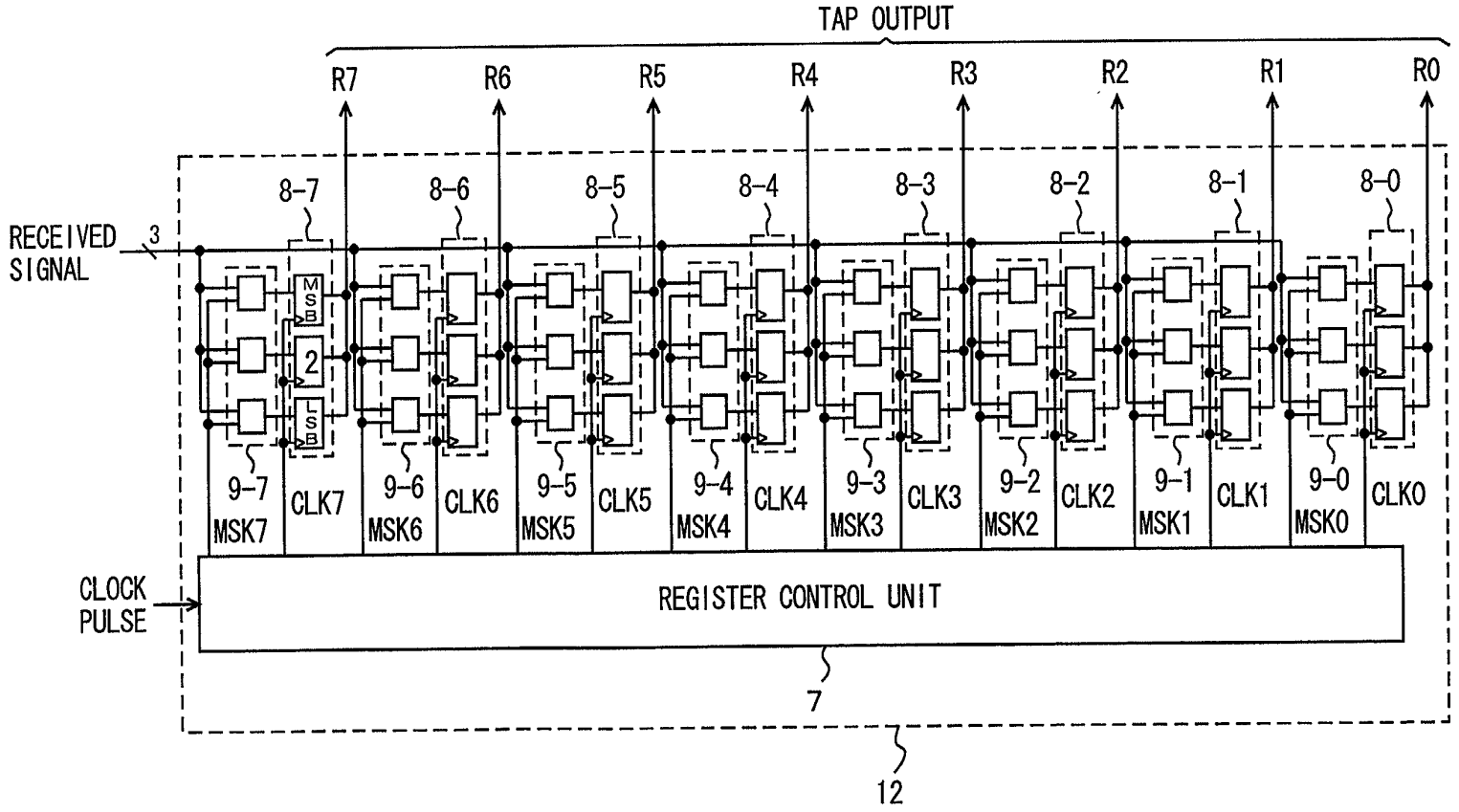

TAP OUTPUT
R7
R6
R5
R4
R3
R2
R1
R0
8-7
8-6
8-5
8-4
8-3
8-2
8-1
8-0
RECEIVED SIGNAL
3
MSB
2
LSB
9-7
MSK7
CLK7
9-6
MSK6
CLK6
9-5
MSK5
CLK5
9-4
MSK4
CLK4
9-3
MSK3
CLK3
9-2
MSK2
CLK2
9-1
MSK1
CLK1
9-0
MSK0
CLK0
CLOCK PULSE
REGISTER CONTROL UNIT
7
12

FIG. 4

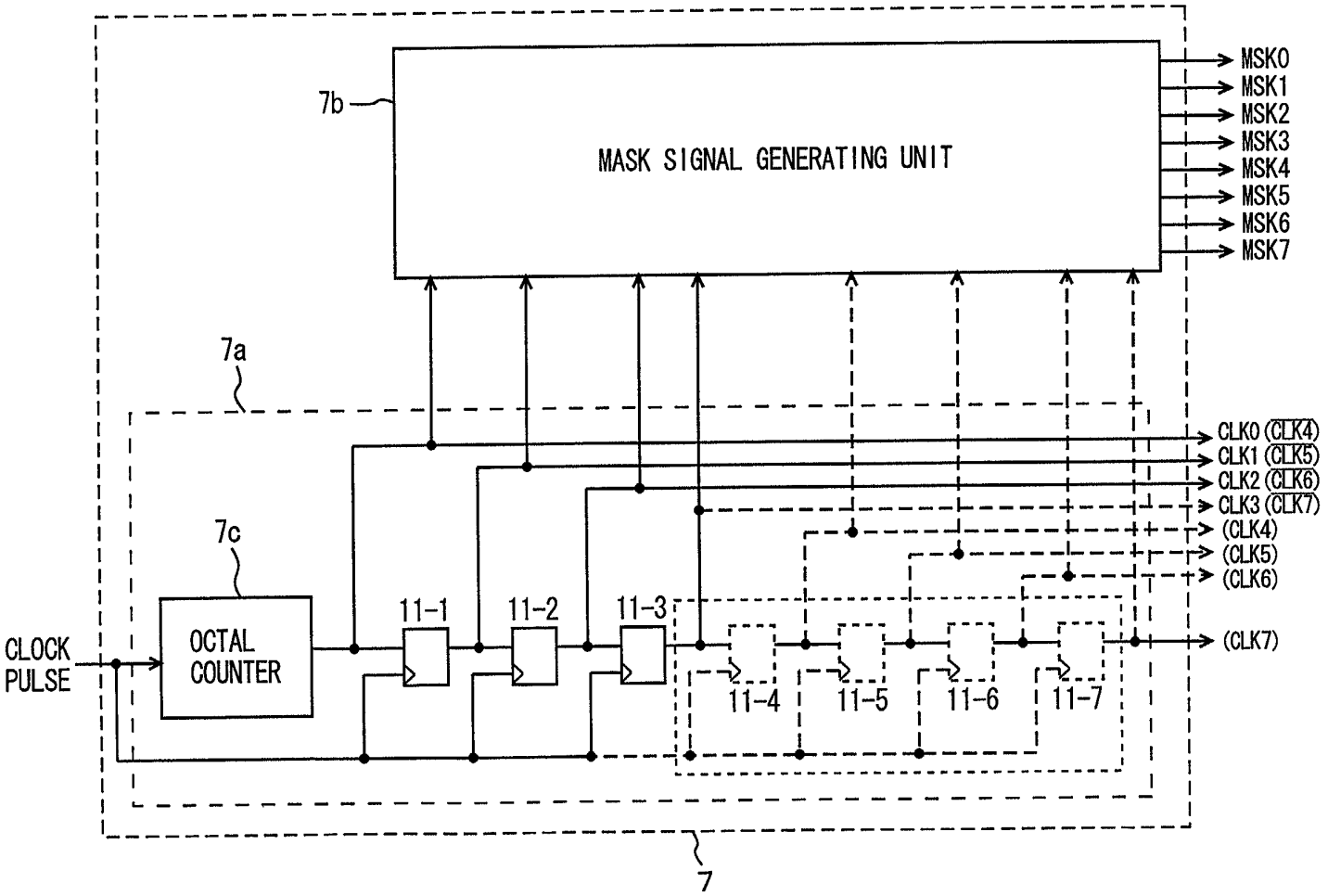

7b
MASK SIGNAL GENERATING UNIT
MSK0
MSK1
MSK2
MSK3
MSK4
MSK5
MSK6
MSK7
7a
7c
CLOCK PULSE
OCTAL COUNTER
11-1
11-2
11-3
11-4
11-5
11-6
11-7
CLK0 (CLK4)
CLK1 (CLK5)
CLK2 (CLK6)
CLK3 (CLK7)
(CLK4)
(CLK5)
(CLK6)
(CLK7)
7

FIG. 5

	INPUT SIGNAL				OUTPUT SIGNAL							
	CLK3	CLK2	CLK1	CLK0	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0
(1)	L	L	L	L	1	1	0	0	0	0	0	0
(2)	L	L	L	H	0	1	0	0	0	0	1	0
(3)	L	L	H	L	1	0	0	1	0	0	0	0
(4)	L	L	H	H	0	0	0	1	0	0	1	0
(5)	L	H	L	L	0	1	1	0	0	0	0	0
(6)	L	H	L	H	0	1	0	0	1	0	0	0
(7)	L	H	H	L	0	0	1	1	0	0	0	0
(8)	L	H	H	H	0	0	0	1	1	0	0	0
(9)	H	L	L	L	1	0	0	0	0	0	0	1
(10)	H	L	L	H	0	0	0	0	0	0	1	1
(11)	H	L	H	L	1	0	0	0	0	1	0	0
(12)	H	L	H	H	0	0	0	0	0	1	1	0
(13)	H	H	L	L	0	0	1	0	0	0	0	1
(14)	H	H	L	H	0	0	0	0	1	0	0	1
(15)	H	H	H	L	0	0	1	0	0	1	0	0
(16)	H	H	H	H	0	0	0	0	1	1	0	0

FIG. 6

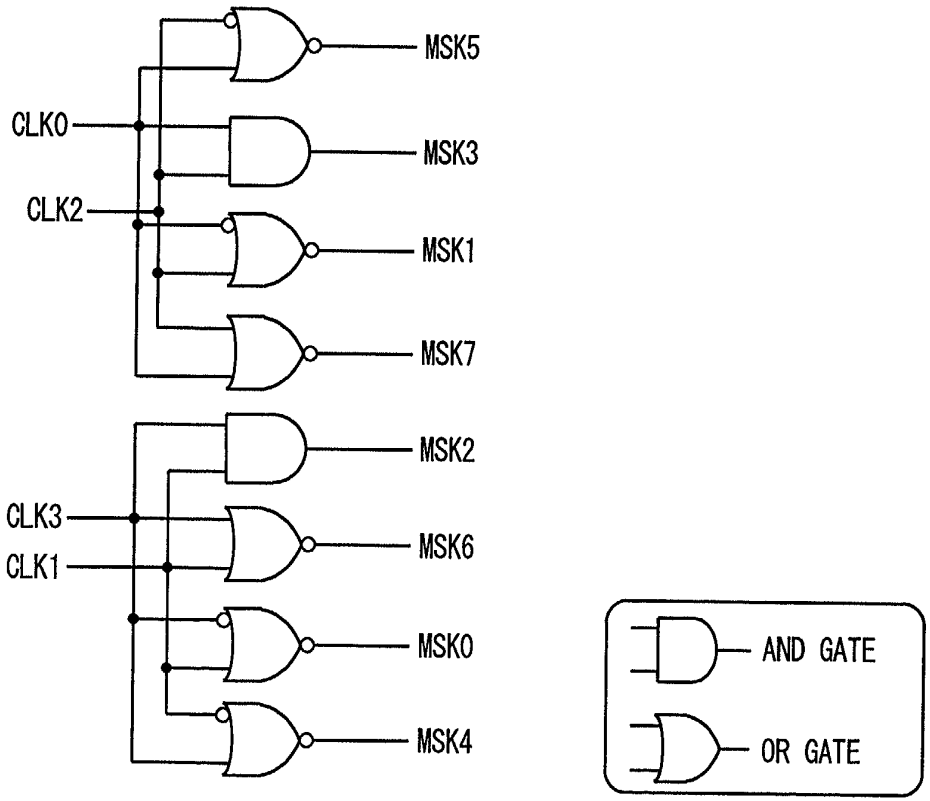

MSK5
CLK0
MSK3
CLK2
MSK1
MSK7
MSK2
CLK3
MSK6
CLK1
MSK0
MSK4
AND GATE
OR GATE

FIG. 7

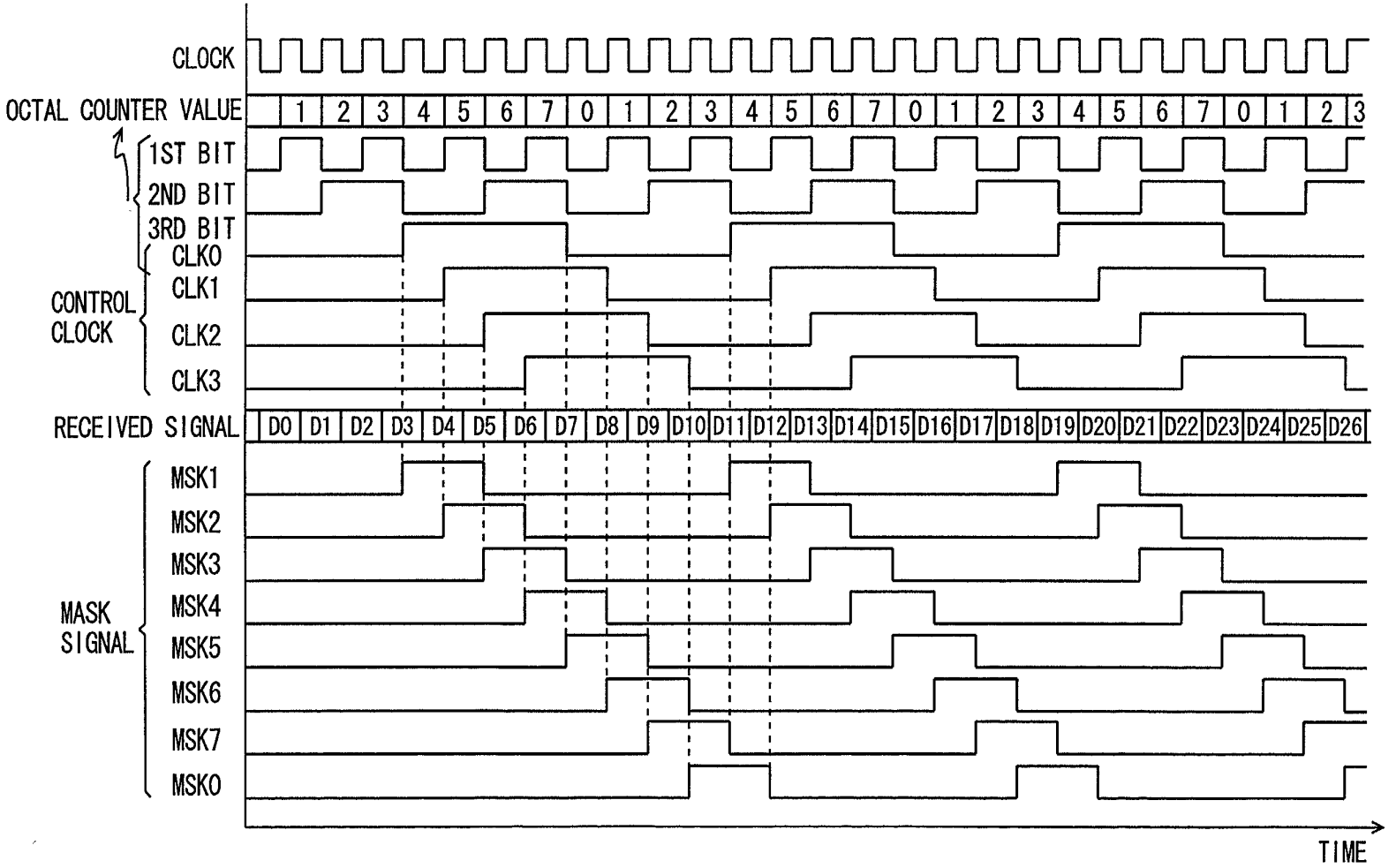

CLOCK
OCTAL COUNTER VALUE
1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3
1ST BIT
2ND BIT
3RD BIT
CLK0
CLK1
CLK2
CLK3
CONTROL CLOCK
RECEIVED SIGNAL
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26
MSK1
MSK2
MSK3
MSK4
MSK5
MSK6
MSK7
MSK0
MASK SIGNAL
TIME

FIG. 8

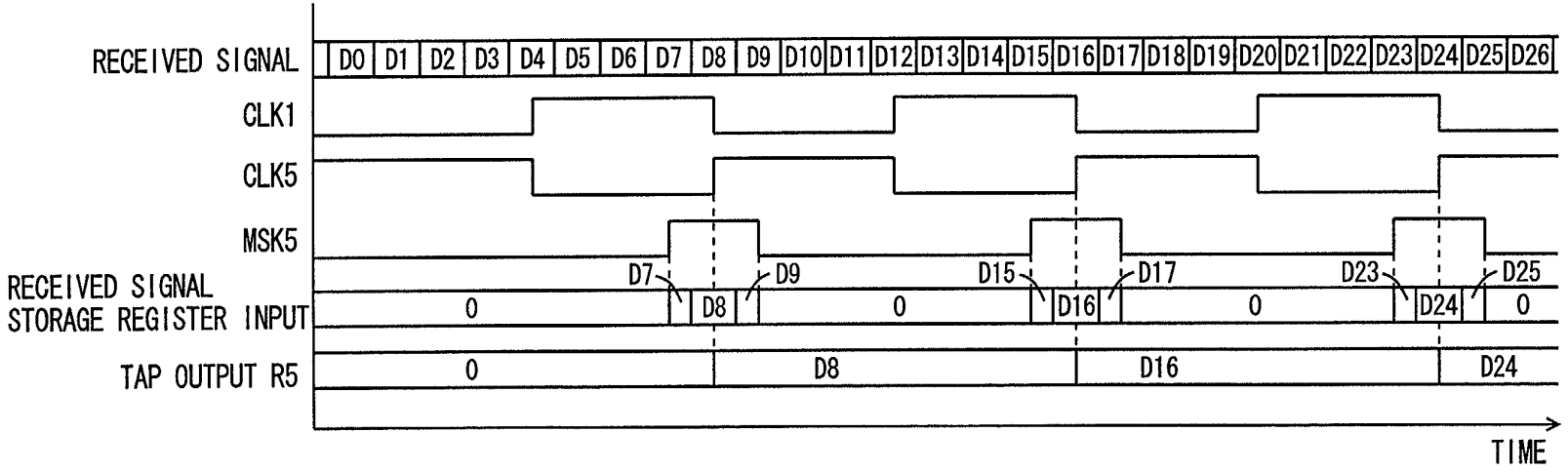

RECEIVED SIGNAL
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26
CLK1
CLK5
MSK5
RECEIVED SIGNAL STORAGE REGISTER INPUT
D7 D9 D15 D17 D23 D25
0 D8 0 D16 0 D24 0
TAP OUTPUT R5
0 D8 D16 D24
TIME

FIG. 9

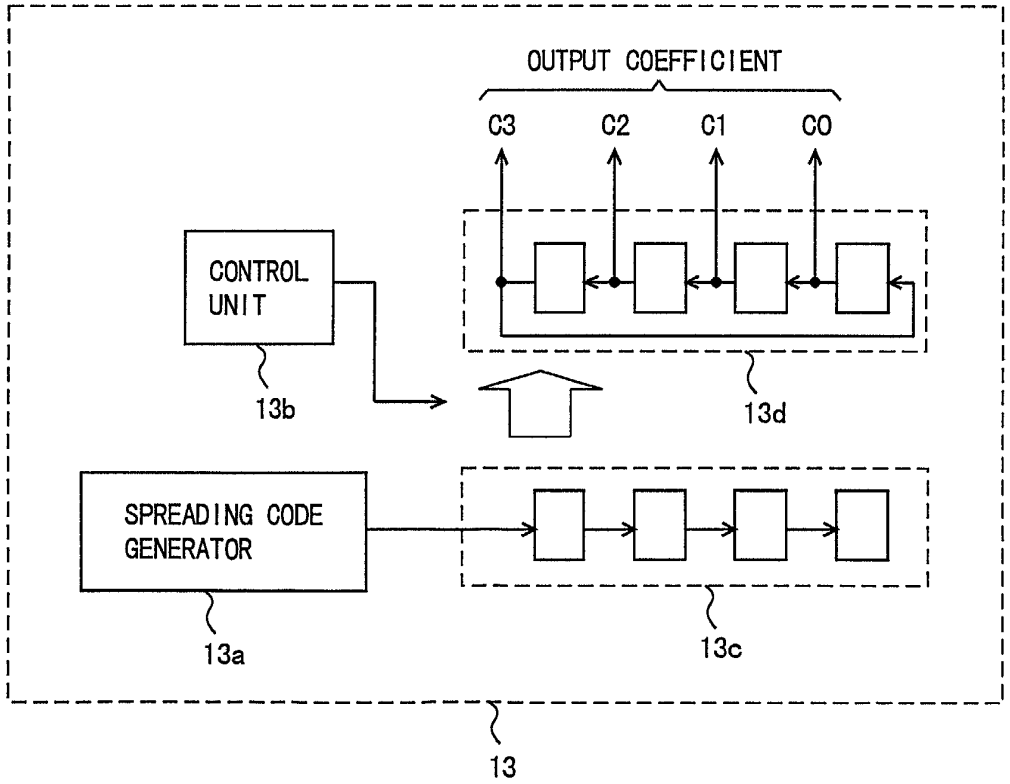

OUTPUT COEFFICIENT
C3
C2
C1
C0
CONTROL UNIT
13b
13d
SPREADING CODE GENERATOR
13a
13c
13

FIG. 10

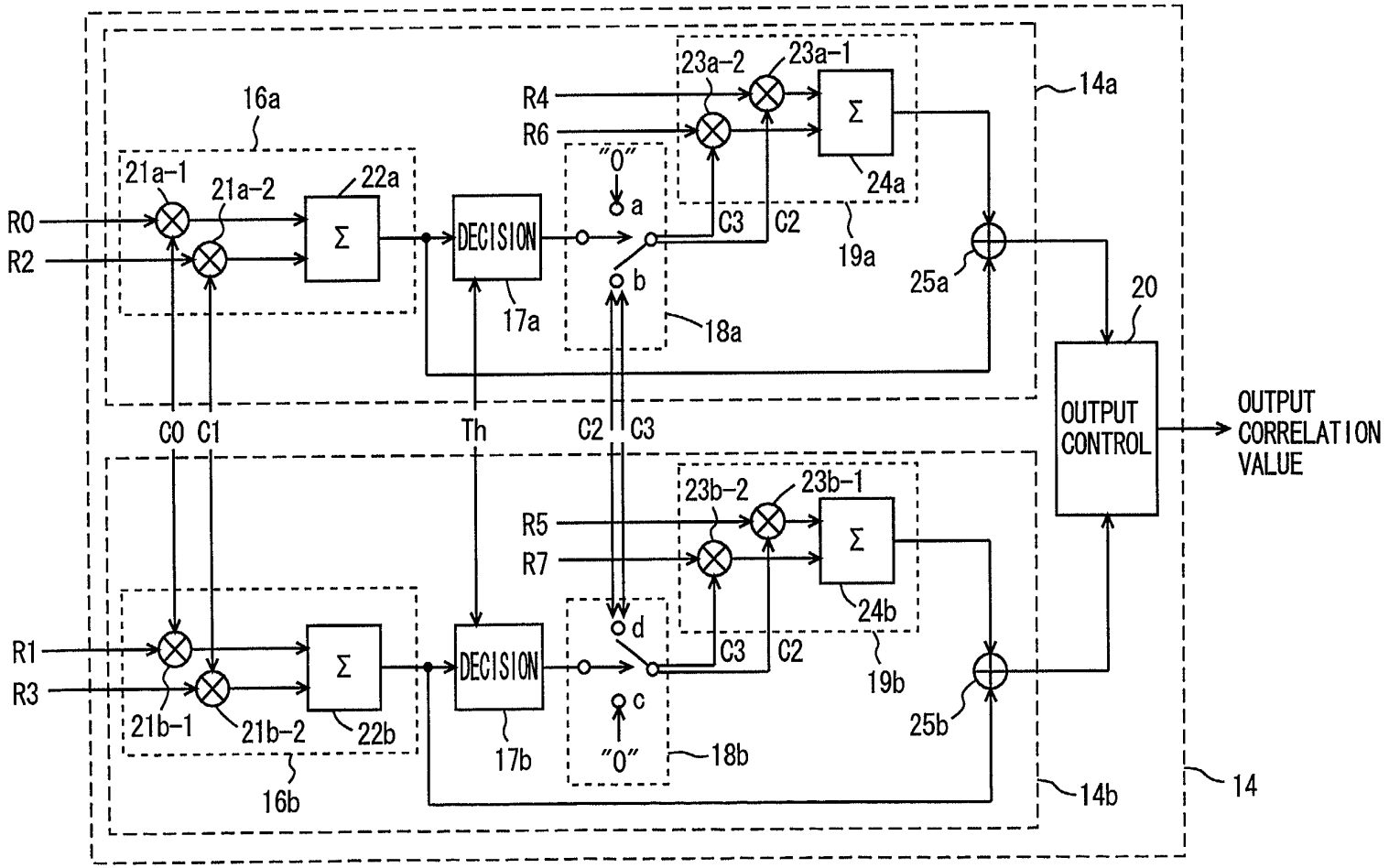

16a
21a-1
21a-2
22a
R0
R2
Σ
DECISION
17a
"0"
a
b
18a
R4
R6
23a-2
23a-1
Σ
24a
19a
C3
C2
25a
14a
20
OUTPUT CONTROL
OUTPUT CORRELATION VALUE
C0 C1
Th
C2 C3
R5
R7
23b-2
23b-1
Σ
24b
19b
d
c
"0"
18b
17b
R1
R3
21b-1
21b-2
22b
16b
25b
14b
14

FIG. 11

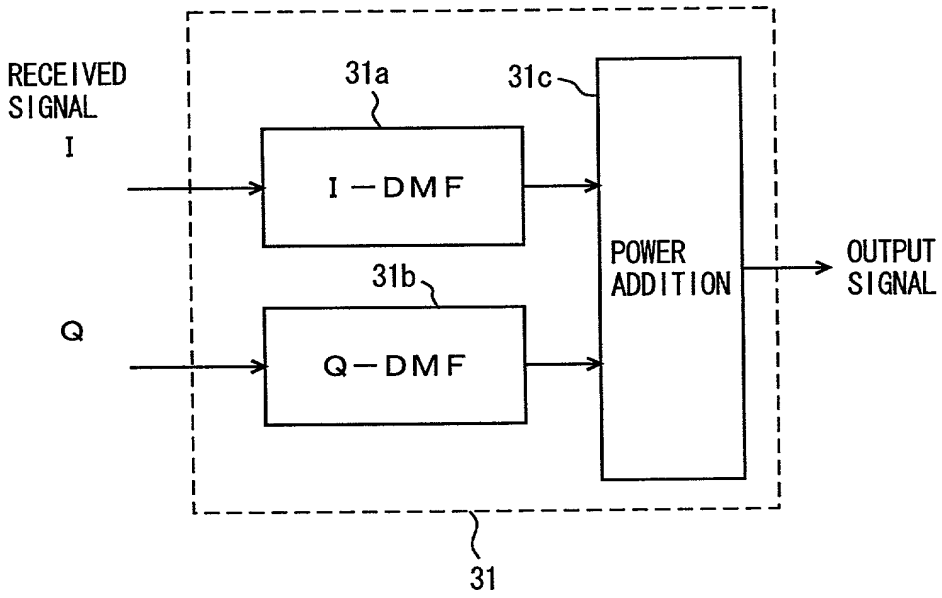
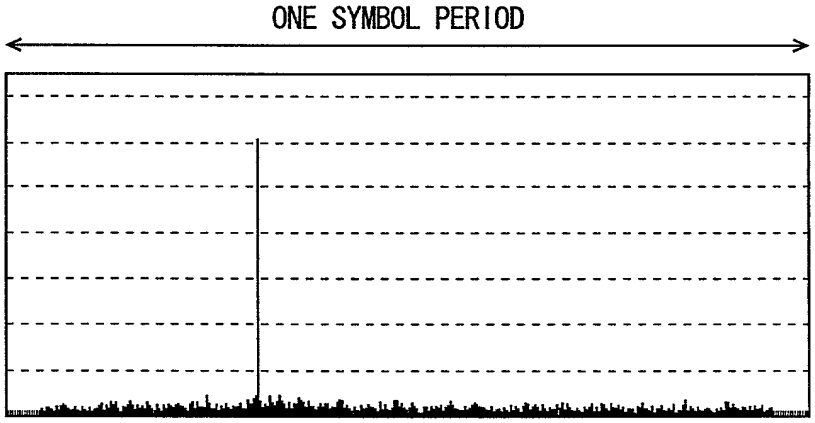
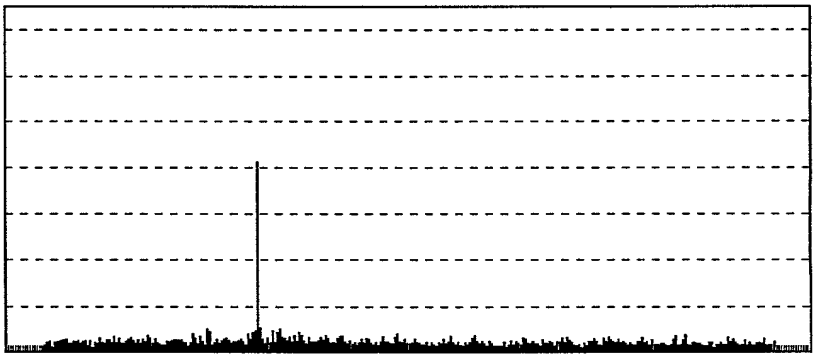

RECEIVED SIGNAL
I
Q
31a
31b
31c
I−DMF
Q−DMF
POWER ADDITION
OUTPUT SIGNAL
31

FIG. 12A



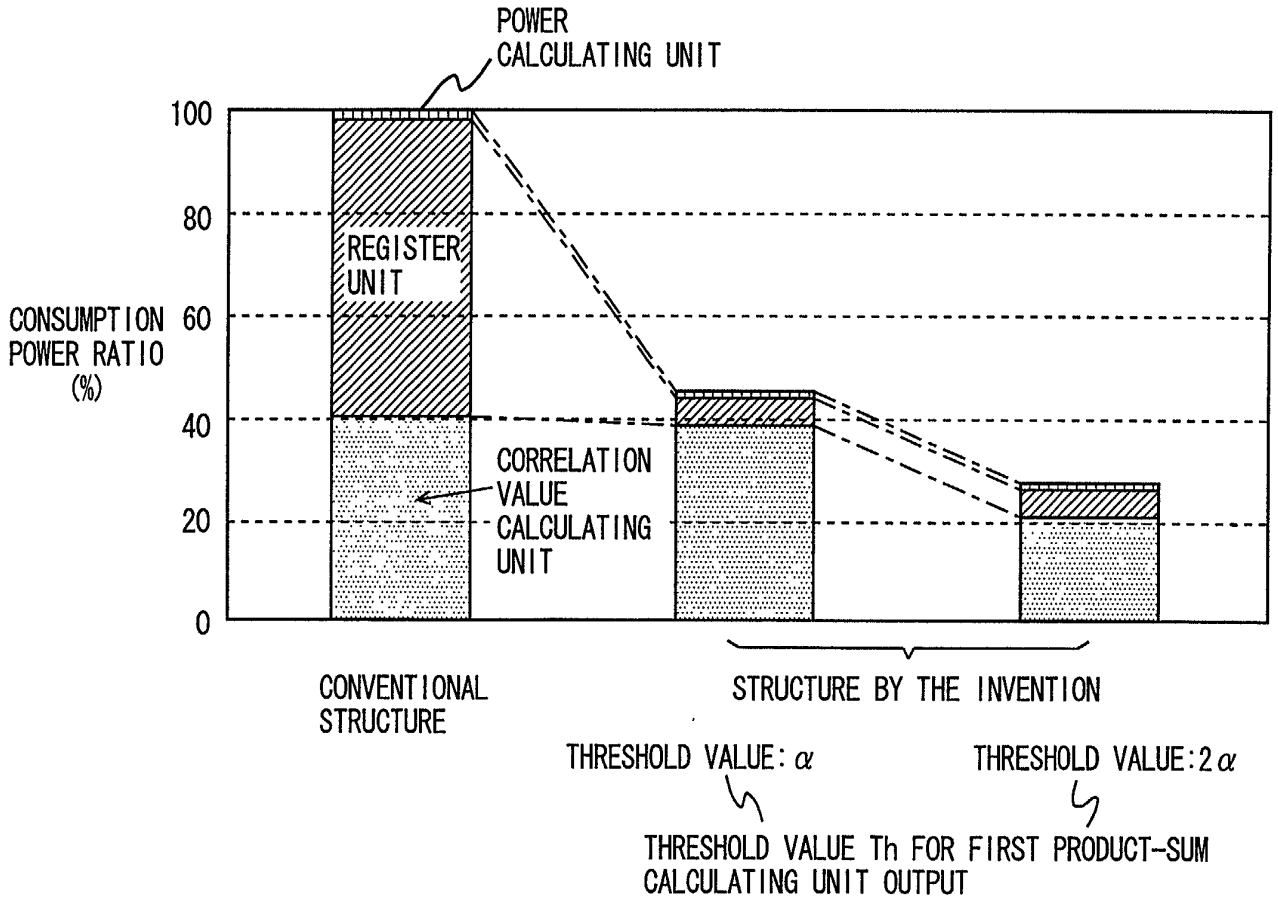
HIGH SNR

FIG. 12B



LOW SNR

FIG. 13


POWER CALCULATING UNIT
100
80
60
40
20
0
CONSUMPTION POWER RATIO (%)
REGISTER UNIT
CORRELATION VALUE CALCULATING UNIT
CONVENTIONAL STRUCTURE
STRUCTURE BY THE INVENTION
THRESHOLD VALUE: α
THRESHOLD VALUE:2α
THRESHOLD VALUE Th FOR FIRST PRODUCT-SUM CALCULATING UNIT OUTPUT

F I G. 1 4 PRIOR ART

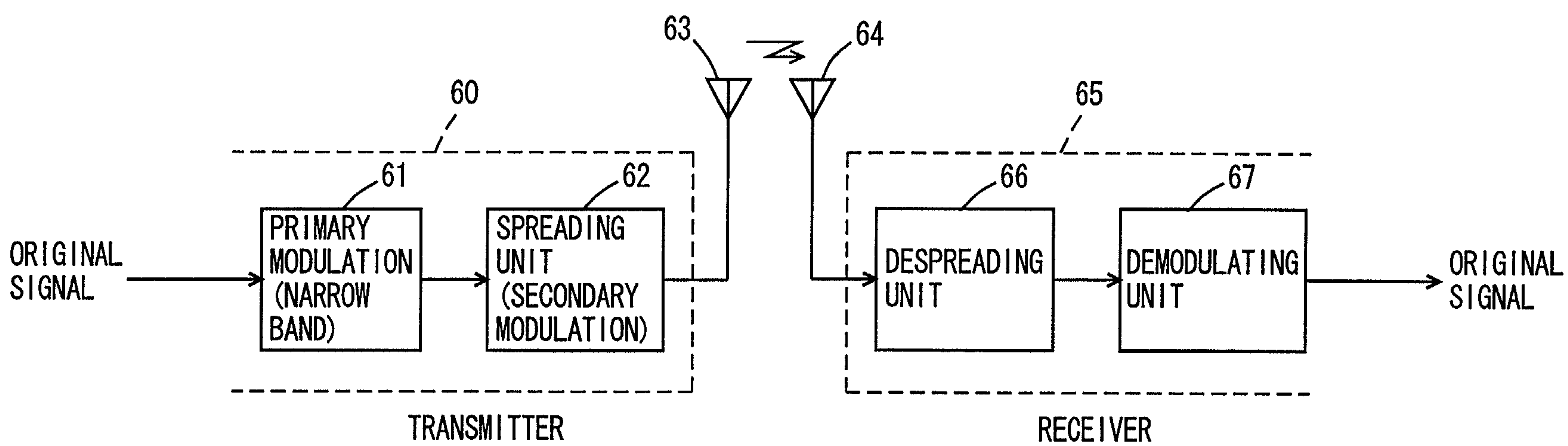


FIG. 15 PRIOR ART

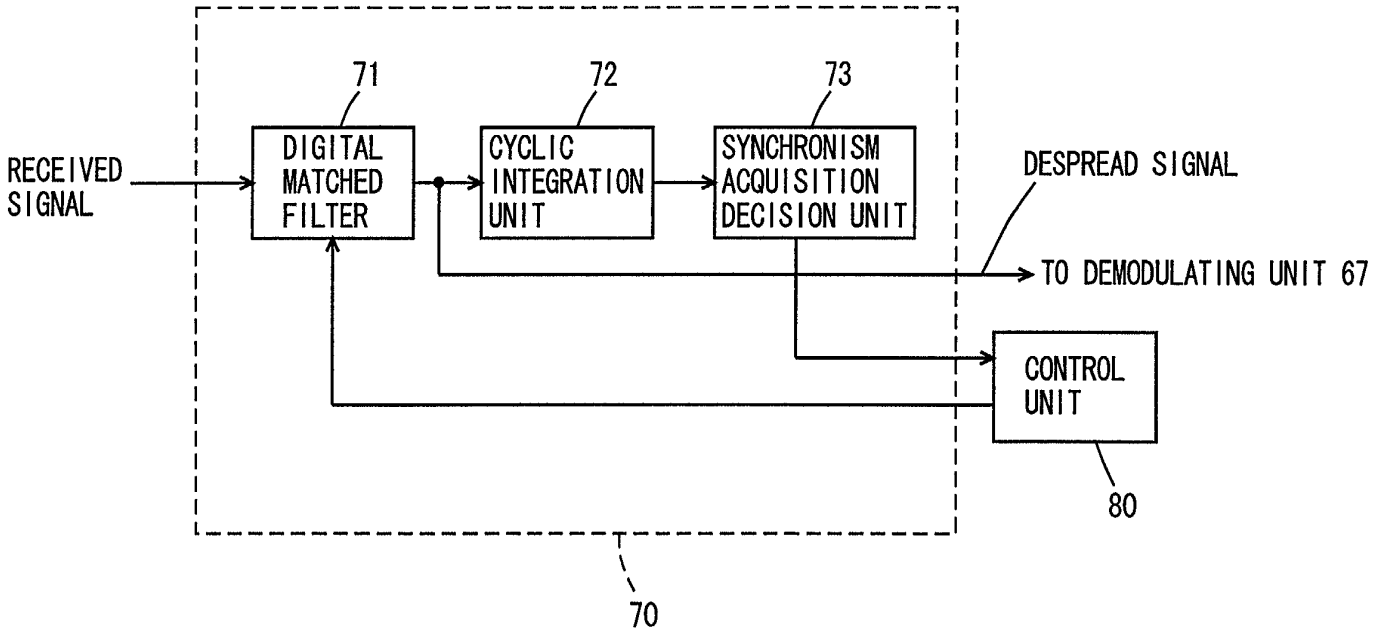


FIG. 16 PRIOR ART